Electronic Version
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Claims

[c1] 1. A method for manufacturing a multi-level SONOS memory cell, comprising:
providing a silicon-on-insulator (SOI) substrate, wherein the SOI substrate comprises a substrate, an insulation layer and a silicon layer;
patterning the silicon layer to form a silicon stripe;
forming a composite dielectric layer over the silicon stripe, wherein the composite dielectric layer is a silicon oxide/silicon nitride/silicon oxide layer, and the composite dielectric layer covers a top part and two sidewalls of the silicon stripe;
forming a conductive stripe over the SOI substrate, wherein the conductive stripe is perpendicular to the silicon stripe;
removing the composite dielectric layer not covered by the conductive stripe;
forming source/drain regions in the silicon stripe beside two sides of the conductive stripe;
forming spacers on the sidewalls of the silicon stripe and the overlapping portion of the conductive stripe and the silicon stripe; and
removing the conductive stripe not cover by the spacers

to form a first control gate and a second control gate on the two sidewalls of the silicon stripe.

[c2] 2. The method of claim 1, wherein after the step of removing the conductive stripe, the composite dielectric layer above the silicon stripe is removed.

[c3] 3. The method of claim 1, wherein the step of removing the conductive stripe further comprises removing the spacers.

[c4] 4. The method of claim 1, wherein the step of forming the source /drain regions comprises performing ion implantation.

[c5] 5. The method of claim 1, wherein the step of forming the composite layer over the silicon stripe further comprises:
forming a first silicon oxide layer over the silicon stripe by thermal oxidation;
forming a silicon nitride layer over the first oxide layer by chemical vapor deposition; and
forming a second silicon oxide layer over the silicon nitride layer by chemical vapor deposition.

[c6] 6. A method for manufacturing a multi-level memory cell, comprising:
providing a substrate;

forming sequentially over the substrate, an insulation layer and a semiconductor layer above the insulation layer;
pattering the semiconductor layer to form a semiconductive stripe;
forming a first dielectric layer over the semiconductive stripe;
forming a charge trapping layer over the first dielectric layer;
forming a second dielectric layer over the charge trapping layer;
forming a conductive layer over the substrate;
patterning the conductive layer to form a conductive stripe, wherein the conductive stripe and the semiconductive stripe are perpendicular to each other;
forming source/drain regions in the semiconductive stripe beside two sides of the conductive stripe;
forming spacers on sidewalls of the semiconductive stripe and the overlapping portion of the conductive stripe and the semicoductive stripe; and
removing the conductive stripe not covered by the spacer to form a first control gate and a second control gate on the sidewalls of the semiconductive stripe.

[c7] 7. The method of claim 6, wherein the step of removing the conductive stripe further comprises removing the

composite dielectric above the semiconductive stripe.

[c8] 8. The method of claim 6, wherein the step of removing the conductive stripe comprises removing the spacers.

[c9] 9. The method of claim 6, wherein the step of forming the source/drain regions further comprises performing ion implantation.

[c10] 10. The method of claim 6, wherein the semiconductor layer is a silicon layer.

[c11] 11. The method of claim 6, wherein the conductive layer is a polysilicon layer.

[c12] 12. The method of claim 6, wherein the charge trapping layer comprises a silicon nitride layer.

[c13] 13. A multi-level SONOS memory cell, comprising:
a substrate, comprising:
a substrate layer;
an insulation layer, disposed on the substrate layer;
a silicon stripe, disposed on the insulation layer;
a first control gate and a second control gate disposed respectively on sidewalls of the silicon stripe;
source/drain regions, configured in the silicon stripe beside both sides of the first control gate and the second control gate; and

a silicon oxide/silicon nitride/silicon oxide layer, disposed between the first control gate and the silicon stripe, and between the second control gate and the silicon stripe.

[c14] 14. The memory cell of claim 13, wherein the substrate comprises a silicon-on-insulator substrate.

[c15] 15. A multi-level memory cell, comprising:
a substrate;
an insulation layer, disposed on the substrate;
a semiconductive stripe, disposed on the insulation layer;
a first control gate and a second control gate disposed respectively on sidewalls of the semiconductive stripe;
source/drain regions, configured in the semiconductive stripe beside both sides of the first conductive gate and the second conductive gate;
a charge trapping layer, disposed between the first control gate and the semiconductive stripe, and between the second control gate and the semiconductive stripe;
a first dielectric layer, disposed between the charge trapping layer and the semiconductive stripe; and
a second dielectric layer, disposed between the charge trapping layer and the first control gate, and between the charge trapping layer and the second control gate.

[c16] 16. The multi-level memory cell of claim 15, wherein the semiconductive stripe comprises silicon.

[c17] 17. The multi-level memory cell of claim 15, wherein the charge trapping layer comprises a silicon nitride layer.

[c18] 18. The multi-level memory cell of claim 15, wherein the first dielectric layer comprises a silicon oxide layer.

[c19] 19. The multi-level memory cell of claim 15, wherein the second dielectric layer comprises a silicon oxide layer.